ABSTRACT OF THE DISCLOSURE

An input circuit includes a data input unit for receiving input data of the input circuit. A data latch unit latches output data of the input circuit. A reset unit resets the data latch unit in response to a first logic level of a first clock signal. A latch enhancement unit enhances the latching operation of the data latch unit in response to a first logic level of a second clock signal that is delayed in phase from the first clock signal. A clock synchronization unit transfers the input data from the input unit to the data latch unit in response to a second logic level of the first clock signal, the clock synchronization unit blocking a feedthrough current that flows through the reset unit, the data latch unit, and the latch enhancement unit when the first and second clock signals are in a first logic level state.